Hybrid Metrology to Measure Unseeable Quantities: Stress Distribution in Miniaturized Transistors by Raman Scattering Spectroscopy

Toshihiko KANAYAMA

Special Emeritus Advisor, National Institute of Advanced Industrial Science and Technology
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Recently, feature size of semiconductor integrated circuits becomes far below 100 nm, and their fabrication requires reliable measurement methods of local material properties capable of nano level resolution. However, it is almost impossible to invent a measurement technique to meet the requirement. Alternatively, we are developing the hybrid metrology: ***i.e.***, the methodology combining suitable measurement methods with precise simulations to estimate values of an unseeable quantity. Here, as an example, we introduce how the mechanical stress distribution in a miniaturized transistor is evaluated using Raman scattering measurements combined with stress simulation and optical propagation simulation.

Introduction

The semiconductor integrated circuit is still keeping the trend of exponential increase in integration density and performance by miniaturization to nm scale and by adopting various new materials. As a consequence, the fabrication process becomes complicated progressively, requiring reliable measurement methods of local material properties capable of nano-level resolution. This requirement is particularly true for development and design of new devices and new fabrication processes. However, it is almost impossible to invent a measurement technique that can characterize material properties of components constituting nanoscale devices in actual integrated circuits hopefully in a nondestructive manner.

Alternatively, to meet the requirement, we are developing the hybrid metrology: *i.e.*, the methodology combining suitable measurement methods with precise simulations to estimate values of an unseeable physical quantity from measurable values (**Figure 1**). In designing semiconductor devices and fabrication processes, computer simulators called technology computer-aided design (TCAD) are frequently used. The TCAD is composed of device simulators to predict operation and performance of devices and process simulators to deal with fabrication processes. The device simulators calculate not only electrical operations of transistors but also heat generation and dissipation arising from device operation, and optical functions such as light emission and sensing. The process simulators estimate such material properties as chemical composition and internal stress in addition to device structures. Thus, it is possible to extend the TCAD to deal with physical processes of a measurement. The extended TCAD will enable us to simulate how a measured value arises from properties of the object, and oppositely to estimate the original properties from the measured quantities. This combination becomes more efficient if several different measurement methods are included in the simulation.

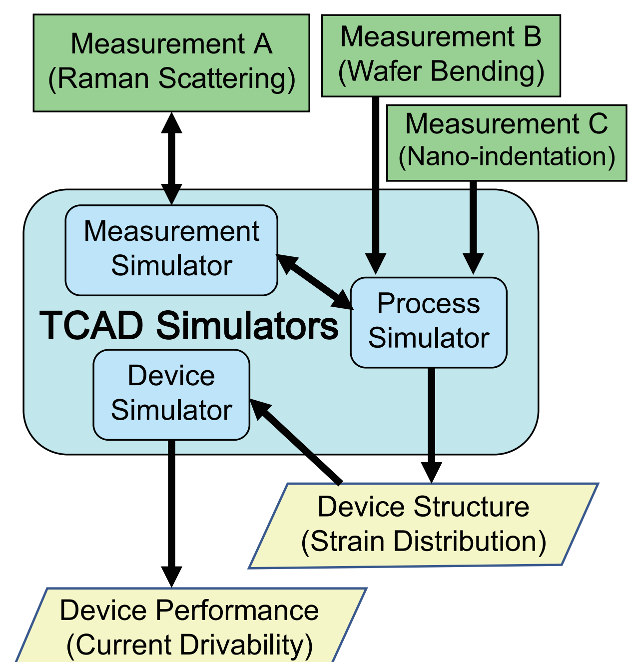

Figure 1 Hybrid metrology uses computer simulations to combine results of different measurement methods to estimate values of an unseeable quantity. Examples are indicated in parentheses for internal stress measurements of miniaturized transistors.

On the other hand, a TCAD simulation cannot start without knowing values of necessary parameters such as device structures and materials. Usually, these values are determined beforehand by suitable measurement methods or from material characteristic tables and given to the TCAD. But, if the TCAD contains a procedure to assess the parameter values with the aid of suitable measurements, the parameter determination becomes more reliable.

In this article, we show an example of our hybrid measurement analyses: determination of mechanical stress distribution in a miniaturized Si transistor using Raman scattering measurements combined with stress simulation and optical propagation simulation. The mechanical stress is now adopted in miniaturized transistors to increase mobilities of electrons and holes and to enhance the drivability of electrical current. Usually, a tensile stress along the channel direction is used to enhance the electron mobility in n-type MOS transistors, and a compressive one is for holes in p-type MOS. This is a very useful method to improve the transistor performance without altering the channel material from Si. However, the mechanical stress is sensitive to many parameters, such as structure and arrangement of transistors, and thus precise measurement and control are required in the design and fabrication. Although there are several possible methods to monitor the stress in transistors, *e.g.*, electron beam diffraction, the Raman scattering spectroscopy is also a possible candidate. The advantage of such optical measurement as Raman scattering is that it allows non-destructive and non-contacting measurements and hence can be versatilely applied to a wide range from development to in-process monitoring. It is also a particular superiority here that the underlying physics is well understood, making the simulation reliable. In contrast, the spatial resolution is limited by the optical diffraction, and cannot reach the 10 nm level necessary for the analysis of miniaturized transistors. Moreover, the transistor performance is controlled by the mechanical stress in the channel region below the gate, but this region is optically inaccessible because it is covered with the opaque gate electrode (**Figure 2**). Accordingly, whether or not the Raman scattering is applicable to the stress measurement in miniaturized transistors depends on how the necessary information is extracted from measurable values with the aid of computer simulations, *i.e.*, the hybrid metrology shown in **Figure 1**.

Raman Scattering Measurement

The Raman scattering is the scattering of light by a matter accompanied with a wavelength shift corresponding to a vibration frequency of constituting atoms. When the scattering object is a stress-free single crystal of Si at room temperature, this amount of wavelength shift, *i.e.*, the Raman shift is 520.5 cm^{-1}, which is equivalent to the optical phonon frequency of Si. If the Si is under a hydrostatic compressive stress, the lattice constant decreases leading to an increase in optical phonon frequency; oppositely, a tensile stress decreases the phonon frequency. Thus, the Raman shift reflects the local stress. However, because the mechanical stress in a cubic crystal is a six-component tensor quantity (three axial components and three shear components), a single value of Raman shift is absolutely insufficient to estimate actual stress. This is particularly true if the stress is anisotropic; in this case, a positive or negative Raman shift does not necessarily mean the stress is compressive or tensile. A possible way for quantitative estimation is to analyze the polarization dependence. In Si, a cubic crystal, the optical phonon is triply degenerated, but if the crystal is under an anisotropic stress, it removes the degeneracy and gives rise to the polarization dependence of Raman shift.

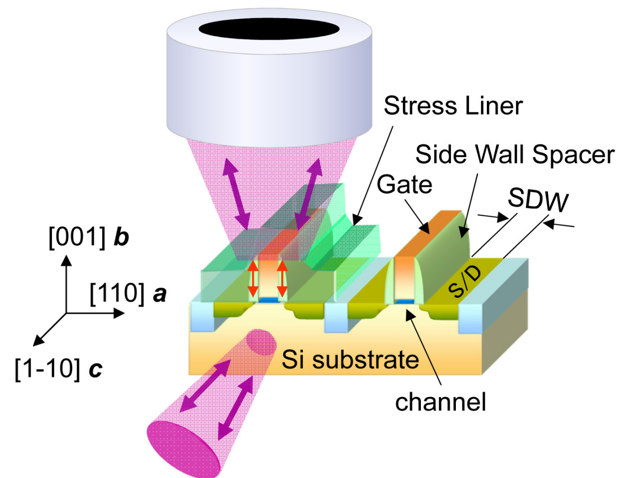

Figure 2 Schematic transistor structure, and two configurations of Raman measurements: vertical illumination / detection, and back scattering on a cleaved cross section. Stress liner is not shown for the transistor on the right. Definition of polarization directions are also shown: a // [110], b // [001], and c // [1-10]. S/D: source/drain, SDW: source drain width.

In actual measurements of Si transistors, we used a confocal Raman microscope in the backscattering configuration equipped with a UV Ar ion laser and an oil immersion micro-objective lens with a numerical aperture of 1.3[1]. The resulting spatial resolution was 150 nm. The polarized spectra were measured with the polarized excitation light and the peak positions were determined by Lorentz curve fittings. The wavelength of the excitation laser beam was 364 nm. This wavelength is near a peak in the reflectivity spectrum of Si, giving high efficiency to Raman scattering. In addition, the penetration depth in Si is only 10 nm. This fact simplifies the analysis procedure by ensuring that the scattered light arises only from the surface regions.

Measurement on a Cross Section of a Transistor

In conventional integrated circuits, MOS transistors are aligned on a [001] oriented Si wafer surface with their channel direction

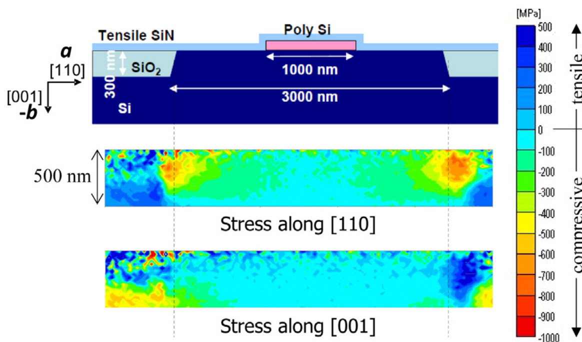

Figure 3 A large n-MOS transistor structure with 1 μm gate length and stress distributions estimated by Raman measurements on a cleaved surface.

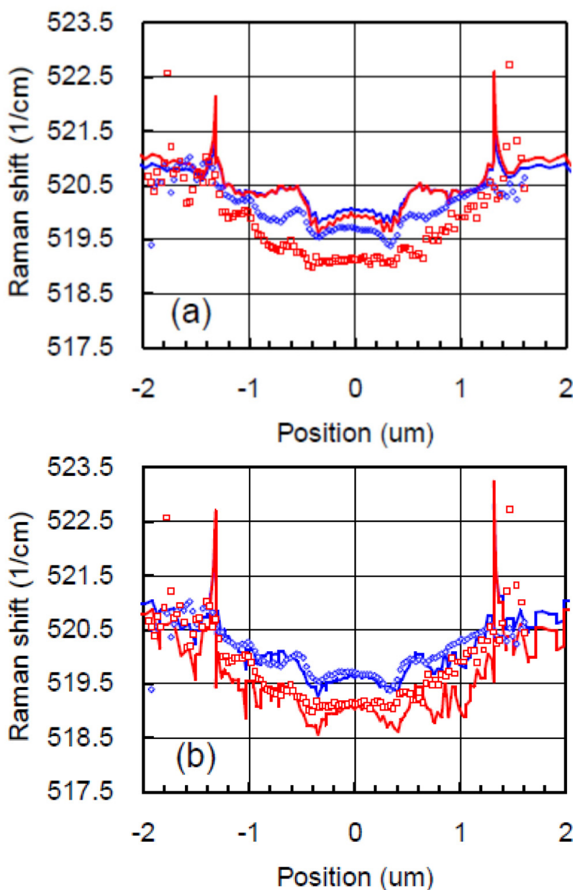

Figure 4 Measured Raman shift data (open square) along the a direction just below the channel surface on a cleaved surface and simulated results (solid line) using internal stress values without calibration (a) and after fitting (b). Blue color indicates the Raman shift of **a**-polarized light and red color is for the one with **b**-polarization both excited by the **a**-polarized light.

parallel to the [110], as shown in **Figure 2**. Thus, the wafer can be cleaved to expose a [1-10] oriented plane perpendicular to the gate, which is available to Raman measurement mapping on a cross section of a transistor including the source, drain and channel regions. **Figure 3** is an actual result of Raman mapping on a cross section of a transistor structure with a 1 μm gate length[2]. This transistor structure is a relatively large test structure to mimic an n-MOS transistor for the purpose of calibration of a stress simulator. The top surface of this structure was coated by a stress liner composed of a Si nitride film to exert tensile stress on the channel region. This figure shows spatial distribution of two stress components directing to [110] and [001] calculated at each measurement position from two Raman shifts, *i.e.*, an **a**-polarized component and a **b**-polarized one both excited by the **a**-polarized light. The calculation can be carried out assuming that other stress components (shear components and the stress perpendicular to the cross section) are negligible. It is seen in this mapping that the major component is a uniaxial compression along the [110] channel direction exerted by the isolation region composed of SiO_2.

For further precise analyses, calibration of stress simulator was conducted in a manner shown in **Figure 4**. This figure shows the Raman shift values on a line just below the Si wafer surface along the direction from the isolation through the source to the drain. The values are compared between the actual measurement and the stress simulation based on a finite element method. Since the stress simulation is very sensitive to the structure, we precisely identified the shape and dimensions of the test structures by transmission electron microscopy. For **Figure 4 (a)**, the stress simulator used the values of internal stress for the Si nitride liner and the poly-Si gate measured by wafer bending for blanket films and the Young's moduli measured by a nano-indenter. Even though, the calculated values do not match the measured ones. This is because the material values used for the simulation were measured for the blanket films and different from the actual values for the films deposited on small structures.

Then, the simulated results were fitted to the measurement results by adjusting such material values as internal stress in the Si nitride film, the poly-Si gate and the isolation SiO_2. As seen in **Figure 4 (b)**, the calibrated simulation reproduces well the measurement results. We acquired material values necessary for the stress simulation by repeating this fitting procedure for several times in a fabrication process of both n and p MOS transistors. In other words, measurements of mechanical properties are achieved for small structure components of transistors, in this way.

Measurement on a Top Surface of a Miniaturized Transistor

The above procedure enables us to measure local mechanical properties and calibrate the stress simulator, but this is a tedious destructive measurement. Furthermore, the overall spatial resolution is limited by the measurement optics, making it impossible to apply the procedure directly to the mapping in smaller transistors. Consequently, we need a method to measure directly a completed miniaturized transistor in a non-destructive manner in order to verify the calibrated stress simulator and to monitor the fabrication process.

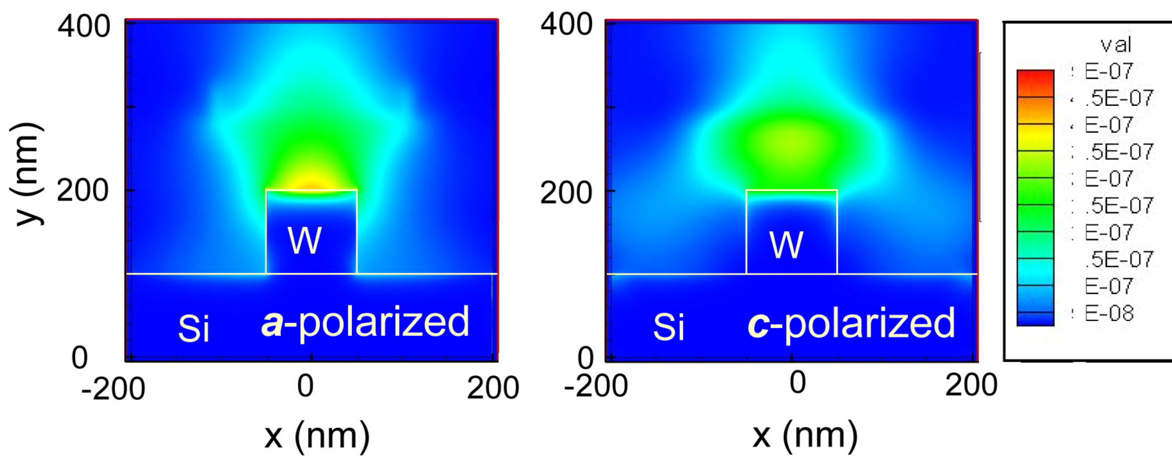

Figure 5 FDTD simulation of incident light intensity around a 100 nm W metal gate for two different polarization directions.

The direct stress measurement is realized by observing what information is obtained from a Raman measurement with the excitation light focused just above a completed transistor gate, as shown in **Figure 2**. As indicated by the red arrows, the only possible propagation route for the excitation and the detection light is through the gate side wall spacer. To get insight about the possibility of this measurement, the light propagation was simulated by a finite-difference time domain (FDTD) method for the case that a light with 364 nm wavelength is focused to a Gaussian distribution of 120 nm half width 70 nm above a W gate with a square shape of 100 nm width and height (**Figure 5**)[3]. The simulation was done for two different polarizations, perpendicular (**a**-polarization) and parallel (**c**-polarization) to the gate. For the **c**-polarization, the incident light is scattered by the top surface of the gate and is unable to reach the bottom of the gate. In contrast, the **a**-polarized light is propagated along the gate side wall to the bottom. Thus, by subtracting Raman measurement data in these two different polarization directions, we can extract the stress value in the Si region just around ~50 nm from the gate[3]. The small transistor structure itself works as a near-field optical component to achieve a detection exceeding the diffraction limit.

The above simulation indicates that the propagation along the gate is enhanced by adopting the perpendicular **a**-polarization for both the excitation and the detection light. The side wall spacer, which is composed of Si nitride transparent for the measurement UV light, has also a waveguide effect because of its relatively high refractive index. The source/drain regions are covered with contact metals and do not contribute to the Raman signal. The entire surface of a transistor is covered by a stress liner film, which is also composed of transparent Si nitride and does not disturb the measurement.

Figure 6 is an actual result of Raman measurement from the top surface of a p-type MOS transistor with 45 nm gate length[2]. Note that the Raman measurement is achieved through the side wall spacer, even if its width is 20 nm, almost 1/20 of the wavelength. This is owing to the waveguide effect of both the gate and the side wall spacer. This figure shows the measured Raman shifts as a function of the source-drain width (SDW, **Figure 2**) in comparison with the values calculated from the stress in the Si region just below the side wall spacer using the stress simulator before and after the calibration stated above. The positive Raman shift from the stress-free value (520.5 cm^{-1}) indicates the presence of compressive stress. The compressive stress decreases as the SDW narrows because the area covered by the stress liner shrinks. As seen, the measured data coincide well with the values calculated by the stress simulator after the calibration. This verifies that the simulator is applicable to smaller dimensions even if the calibration was done for a 1 µm gate transistor structure. Actually, we calculated the stress value in the channel region below the gate by the calibrated stress simulator, and transferred the value to a device simulator to predict the electrical performance of the transistor. The simulated result agreed well with the measured performance of the actual transistor.

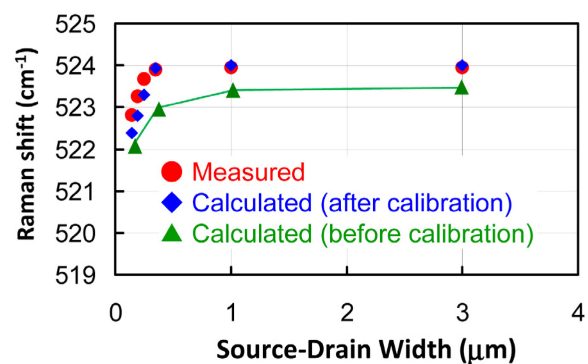

Figure 6 Raman shift measured by the vertical illumination and detection configuration through side wall spacer in a p-MOSFET with 45 nm gate length as a function of source-drain width (SDW in **Figure 1**). Measurement results (red) are compared with simulated results before (green) and after (blue) calibration using the data obtained by cross sectional measurements.

Conclusion

Nowadays, the computer simulation is widely used in various metrology, *e.g.*, to improve spatial resolution, or to reconstruct three-dimensional images. As shown above, if a measurement method is combined with a CAD simulator for the measurement object, such as TCAD for transistors, then it enables us to reliably estimate values of an unseeable quantity using actual measurement data. We are pursuing this computer-aided hybrid methodology for scanning tunneling microscopy of dopant and carrier concentration profiling in miniaturized transistors[4] as well as the stress measurement shown above. We believe that this hybrid metrology certainly meets the increasing requirements in many scenes in semiconductor technology. This purpose needs a versatile TCAD system easily extendible to new physical models. This is why we are developing our own TCAD system, the Impulse TCAD[5]. This Impulse TCAD is now open to external users[6], whoever are willing to utilize and expand its ability. I hope that this article encourages many readers to attempt the use of the hybrid metrology and the Impulse TCAD for their own purposes.

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