Latest Device Processes and required sensing & control technologies in Semiconductor Chip Manufacturing

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In current and future semiconductor wafer manufacturing, CVD (Chemical Vapor Deposition)/ ALD (Atomic Layer Deposition) and Dry Etch are becoming key technologies. These technologies are utilized increasingly and are widely implemented due to feature size reduction and 3D structures requirements. In addition, there are Multiple competing requirements that are difficult to realize without these technologies but they are still insufficient and far from maturity. Therefore, the performance and capabilities of these technologies must be continuously improved. An innovative process sensing system and a fluctuation-free gas supply offer promising means to improve performance. In order to achieve this, collaboration and close development between equipment users, equipment suppliers, subsystem OEM (Original Equipment Manufacturer), and system solution providers is required and should be maintained.

Introduction

Research and development of semiconductors, as stand-alone devices, originated in the 1940s. Their performance began to improve dramatically, owing to the invention of integrated circuits (abbreviated as IC) in the 1960s, allowing their use in data memories and logic processors. In the 1970s, MOS memory ICs achieved capacity improvement, microscaling and price reduction. This was triggered by introduction of a memory device called dynamic random access memory (DRAM), which has a simple structure consisting of a transistor and a capacitor. Since then, conventional bipolar ICs have come to be used primarily for logic processing purposes. After the 1980s, Japanese electronic manufacturers led the development of DRAMs and dominated the world marketplace by making significant achievements in memory capacities that quadrupled in two years. Moreover, flash memory, a type of non-volatile memory, emerged in the industry in the middle 1980s. Since that time both volatile DRAM and non-volatile flash memory have been used for memory purposes. In the 1990s, South Korea and Taiwan entered the market and many Japanese electronic manufacturers subsequently withdrew after 2000.

For logic processing applications, bipolar ICs have long been used because of their superiority in device speed. However, since bipolar ICs are less advantageous in terms of power consumption and microscaling, the development of MOS ICs accelerated since the 1990s. MOS ICs advanced to almost the same performance as bipolar ICs in the late 1990s, while bipolar ICs, which consume hundred times more power than MOS circuits, are rarely used today except in special applications. Consequently, MOS ICs have been used for both memory and logic processing applications since 2000, enabling sharing of technology for production process development across the two device types, as well as shared or diverted use of production lines.

As described above, microscaling of devices has steadily advanced. However the late 2000s development of microscaling technology slowed and device performance did not advance as rapidly due to physical feature sizes, making it difficult to maintain the speed of development that previously allowed microscaling to 70% in two years (on a one-dimensional basis, i.e. 50% in square measure). Although device manufacturers are striving for R&D breakthroughs, only three or four of them are likely to survive the competition that requires such a large scale investment. It also should be noted that the key process technologies currently sought by these device makers includes atomic layer-based techniques, namely, atomic layer deposition (ALD) and atomic layer etching (ALE). These technologies were developed in the late 1970s and early 1980s but were not applied in the mainstream DRAM technology due to throughput and other reasons. Meanwhile, the minimum feature size of devices shrank dramatically from several dozen microns to several dozen nanometers (10-20 nm) in the period from the 1970s until today. Based on the background of semiconductor development, this article discusses and proposes future directions to be taken by suppliers of manufacturing equipment and functional components.

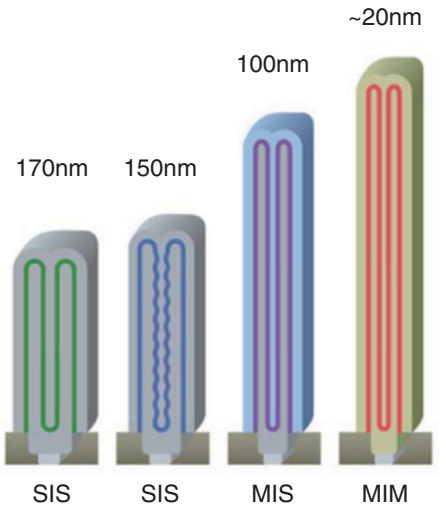

Figure 1 Trend of Storage Node in DRAM

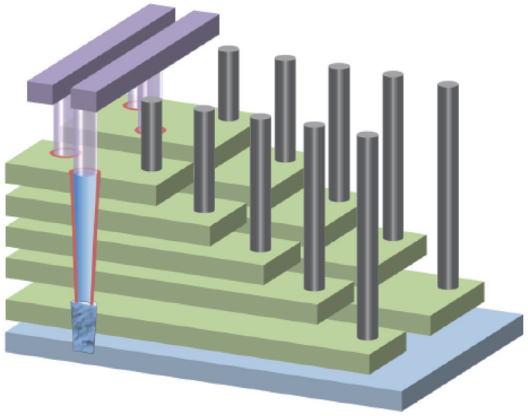

Figure 2 Schematic Diagram of Multi Layer Structure in 3D-NAND

Device and process development

The biggest issue in the microscaling of DRAMs is how to ensure sufficient capacity for storage nodes in which electric charge is accumulated. As microscaling inevitably led to the reduction of the area available for storage nodes, DRAM devices became the first to adopt three dimensional designs. Trench architecture, deep trenches formed on a Si substrate, was previously studied along with stack design, however, cylinder-type DRAMs are mainly used at present. Today insulating films used for capacitance storage are mostly made of materials with higher dielectric constants (high-k material); nitride films, Ta_2O_5 films and ZrO/AlO/AlZrO laminated films compared to oxide films that were previously dominant. Also, as shown in Figure 1, more and more storage nodes use a metal-insulator-metal (MIM) structure as metals replace Si for electrodes. No room for further development has been expected in terms of microscaling and material engineering since 2010 and there is even a move to consider shifting to new memory devices.

In the field of flash memory, solid state drives (SSDs) are now replacing conventional hard disk drives (HDDs) thanks to their increased storage capacity. Microscaling allowed memory capacity expansion until 2000 when a new technique allowed a single memory device can be used to store multiple data like 000~111 rather than a single 0/1 value. The technology, called multi level cell, currently allows memorization of 3 bits/cell (eight levels) at the maximum. In addition, studies are underway to expand the capacity of flash memories by introducing 3D-NAND, a layered structure illustrated in Figure 2. Note that the actual number of layers of a 3D-NAND memory ranges from 32 to 64.

As for the development of logic devices, in the 1990s focus was placed on the microscaling of transistors and the introduction of Cu wiring and low-k dielectric films in the wiring process for the purpose of preventing transmission delay. After 2000, improved performance of transistors encouraged the use of new transistor structures across different generations. Until 130-nm generation, microscaling of two-dimensional structure had been the only means to achieve better performance, lower power consumption, and higher degree of integration and to avoid an increase in the number of transistor formation processes. After the generation of 90-nm devices, a speed improvement technology, strained Si, was adopted. Moreover, materials used for gate and insulator films were gradually replaced in 45-nm and subsequent nodes, resulting in a shift from Si/Si oxide film gate stacks to metal/high-k gate stacks and allowing a wider variety of metal materials to be broadly used in device production processes. During that time, a production technique called the replacement gate method came into use due to the difficulty in performing dry etching on metal/high-k gates and for the purpose of reducing damage to the underlying device area. The new method involves the processes of: (i) poly-Si patterning, (ii) formation of insulator film, (iii) planarization by chemical mechanical polishing (CMP), (iv) low-damage removal of exposed poly-Si, (v) high-coverage deposition of metal/high-k material into the area where poly-si was removed, and (vi) further planarization. Furthermore, more and more devices after the 22-nm generation are likely to adopt FinFET (field effect transistor) technology, which is based on a three-dimensional structure. The nano-wire structure illustrated in Figure 3 would possibly be adopted for 7-nm and later devices, although other various structures are still being studied as well.

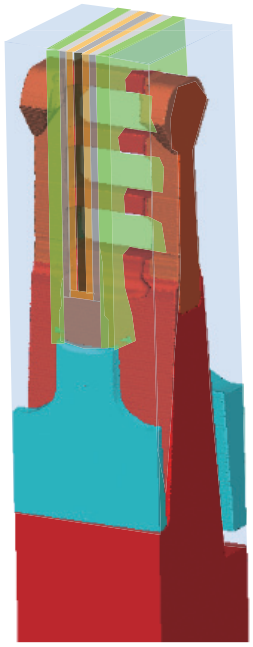

Figure 3 A candidate structure of the next Logic Devices(Nano-Wire)

Device and process technologies of greater importance

The facts mentioned above indicate that device structures have been getting more complex and microscaled year by year, with their aspect ratio gradually increasing. This section gives a brief summary of production process technologies that play key roles in realizing these device configurations.

Let us begin with film-forming technology to form the required type of film on each semiconductor wafer. Low pressure chemical vapor deposition (LP-CVD) was conventionally used in many processes. After 2000, however, there emerged several issues associated with the method, i.e., prolonged heat treatment time and poor step coverage of high-aspect-ratio patterns. Therefore, atomic level deposition (ALD), a technique to form a film with good step coverage at low temperature, gradually came into wider use. Figure 4 shows the principle of ALD. Basically, the newly adopted film-forming method is similar to LP-CVD in that the film is produced as a result of chemical reaction between sources A and B. However, unlike LP-CVD that is based on the deposition of the film material produced in midspace, ALD introduces two sources separately in terms of time. More specifically, a single-layer film consisting only of the A source is deposited first, and then a single reaction layer is formed by supply of the B source. Even with its low film-forming speed compared to LP-CVD, the practical applicability of ALD in production processes has been sufficiently enhanced these days, owing to microscaling that requires reduced film thicknesses. Since the reaction takes place on the surface of a wafer, the film can be formed homogeneously and uniformly at any part of the geometry. Furthermore, recent moves to commercialize a newly developed plasma-based ALD variant called plasma enhanced ALD (PE-ALD) will gradually increase in the number of processes using ALD. Meanwhile, the technology of ALD currently applied for mass production seems to be different from ALD in a strict sense because it is not based on the state of perfect surface saturation.

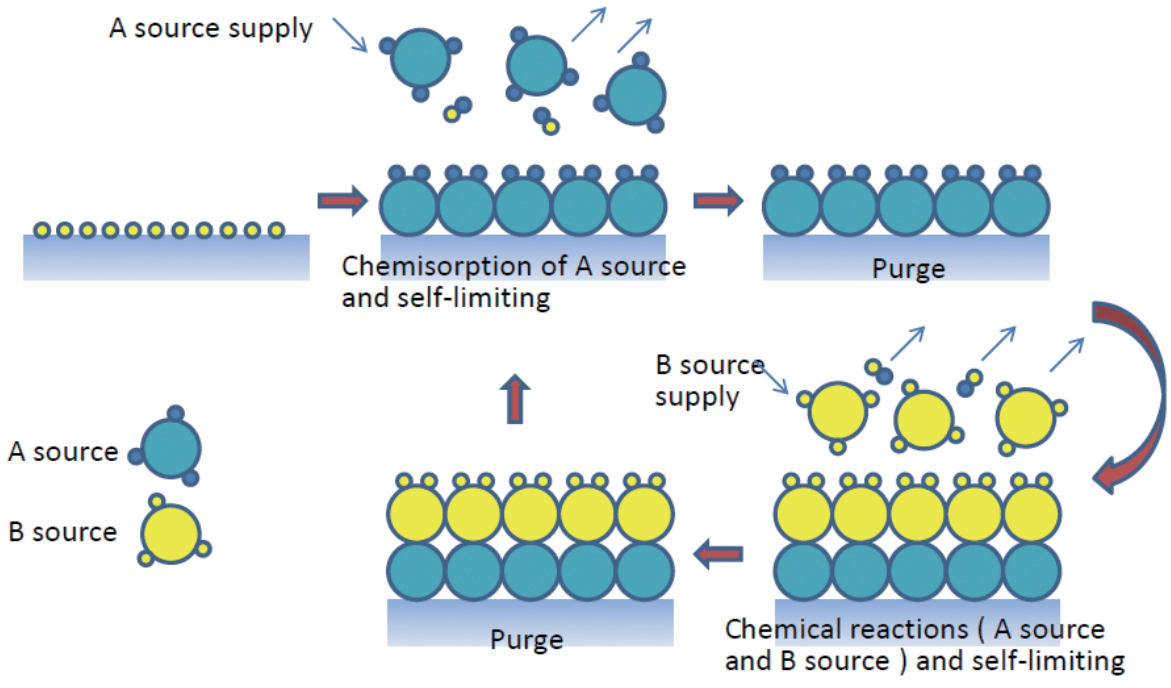

Figure 4 Principle of ALD Technology(Cyclic Process of 4 Steps)

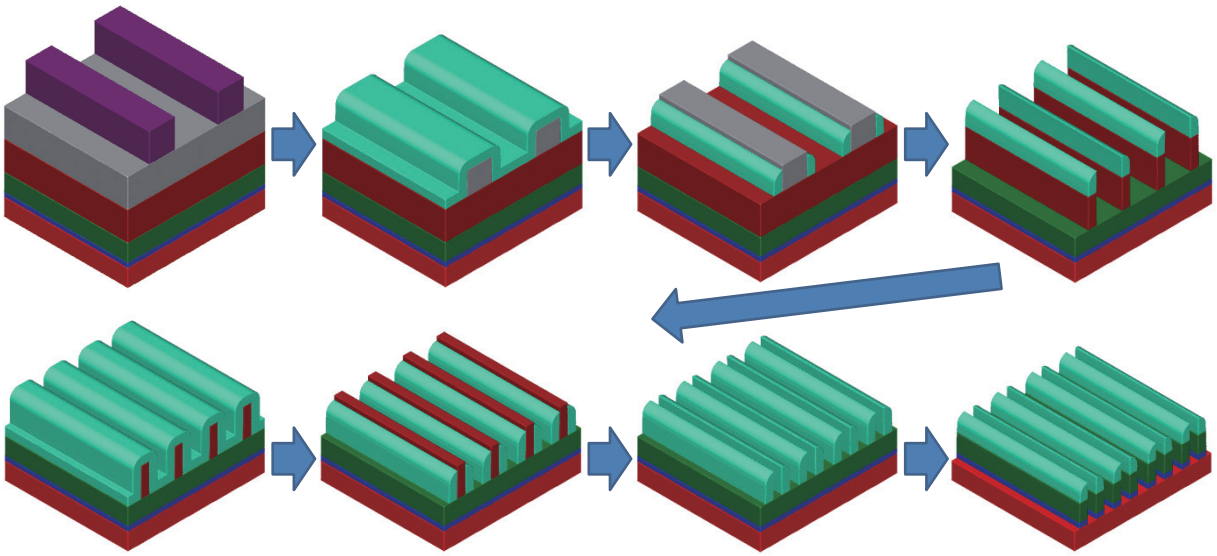

Figure 5 Process Flow Example of SAQP

Next, take a look at planarization technology. As mentioned in Section 2 of this article, the wiring material switched from conventional Al-alloy film to Cu film. This consequently led to a significant improvement of planarization technology in the field of production engineering; in other words, the requirement of adopting Cu film for wiring urged the establishment of CMP technology. Wiring patterns were conventionally produced by: (i) deposition of an Al-alloy interconnecting film on the whole surface of a wafer, (ii) application of patterned masking material, and (iii) removal of only unnecessary portions of the film by using dry etching equipment. On the other hand, Cu wiring is formed using a process called damascene wiring, because dry etching of Cu film is very difficult. The process consists of: (i) dry-etching of insulator film to form slits and hole patterns on it, (ii) deposition of Cu film on the whole surface of the wafer, (iii) introduction of an abrasive called slurry between a polishing pad and wafer, and (iv) chemical and mechanical polishing of the deposited film to remove unnecessary portions. CMP processes are now much more stable compared to they used during early development stages, and CMP equipment is apparently extendable over several generations.

Lithographic exposure is the most important process technology affecting microscaling. The reduced projection exposure method is generally used: a circuit pattern formed on a reticle is reduced in size and resolved on a photosensitive material applied on the surface of the wafer. Since the resolution of patterns heavily depends on the light source wavelength of the stepper used, shorter wavelengths and larger numerical apertures (NA) have been pursued. After 2000, cutting-edge steppers used ArF lasers rather than conventional KrF lasers; however, a significant delay occurred in the development of a promising next-generation light source called EUV, almost preventing further progress of microscaling technologies. To tackle the problem, another technique called the immersion method was put to practical application, which uses liquid enclosed between the stepper lens and wafer to improve resolution by increasing the refraction index. In addition, the life of existing microscaling technology has been significantly prolonged, thanks to a technique called double patterning, which is also known as self aligned double patterning (SADP); a film with desired thickness is formed on an initial pattern produced, and then etched back by means of dry etching in order to obtain the secondary pattern lines of the desired size (actually about half of the initial one) on the sides of each initial pattern line. Moreover, the self aligned quadruple patterning (SAQP) technique, involving a further repetition of SADP to obtain a pattern scaled to a fourth, is currently on the way to practical application. Cost per wafer incorporates the expense required for realization of these production processes, and increases by several percent per for these newly added processes. Furthermore, it should be recognized that the method can be applied only to repetitive patterns and requires trimming of pattern edge by means of dry etching. Figure 5 shows the process flow of SAQP. Size and alignment precision almost entirely depends on the ALD film forming method and the dry-etching technique.

Lastly, importance of the dry-etching technology will be discussed below. Around the year 2000, the process was deemed as an easy-to-use production method that has no major issues except for uniformity and reproducibility. However, because of the subsequent microscaling and adoption of three-dimensional designs, dry-etching technology is now required to deal with extremely difficult tasks such as: (i) etching for SADP (requiring high

dimensional precision and low process cost), (ii) etching for highly selective removal of poly-Si with low damage, and (iii) highly selective vertical etching at vertical portions of a highly stepped under layer, all done without leaving etching residue. Apparently, there are many problems to be solved with regard to the technology. Moreover, isotropic etching with high selectivity is also needed for next generation devices while ALE techniques are increasingly being studied as well.

In total, among the four process technologies mentioned above, ALD film-forming and dry-etching are the technologies that should be significantly improved in the future, as they seem to be far from perfection in terms of both equipment and production processes.

Required measurement and control technologies

As mentioned above, ALD and dry-etching are the key technologies for device processing in the future. A closer look at the equipment and processes currently used for ALD and dry-etching reveals a number of inadequacies in terms of stability and reproducibility. For example, there is a defect called "first wafer effect," which means a series of anomalous results delivered by several wafers processed right after the start of production. It takes place in various situations, causing yield reduction and eventually affecting mass production of semiconductor wafers. Figure 6 shows the relationships among three elements of a production process, taking dry-etching as an example. One of these elements is Equipment Settings, which are usually called as recipes. Another element is the Treatment Environment in which wafers are actually processed. This element is determined by disturbing factors such as chamber internal temperature and deposition substances. The other element is Wafer State, the result of the process each wafer underwent in the treatment environment. If the impact of disturbing factors is too large, the process can hardly control the wafer state in accordance with equipment settings. ALD and other CVD-based techniques, as well as dry-etching, are relatively susceptible to disturbing factors. To keep the wafer state constant in such a processing system, sensing and feedback of the actual treatment environment and wafer state is essential. This is the basic idea of Advanced Equipment Control/ Advanced Process Control (AEC/APC) which has been actually promoted for 20 years.

Figure 7 shows the possibilities of sensing in actual etching equipment. Issues have been identified in respective sensing functions; of these, the plasma emission sensor is the only device used in the actual production equipment at present, with its purpose limited to the determination of the dry-etching end point.

(1) Luminescence and interference sensor (Emission & interferometric sensor): The instrument is capable of measuring the changes in film thickness on the wafer, as well as the dimensions of repetitive patterns, however its application is limited due to the location dependence of measurement at the wafer top requiring movability and a large transmissive window.

(2) Video camera: This device can be used for the same purpose as item (1) and also for monitoring of the overall situation of the wafer, but has not been applied due to issues concerning installation of a transmissive window and a great amount of data needed to be analyzed.

(3) Mass spectrometry (Q-mass analyzer): This type of analysis can determine the atoms and molecules

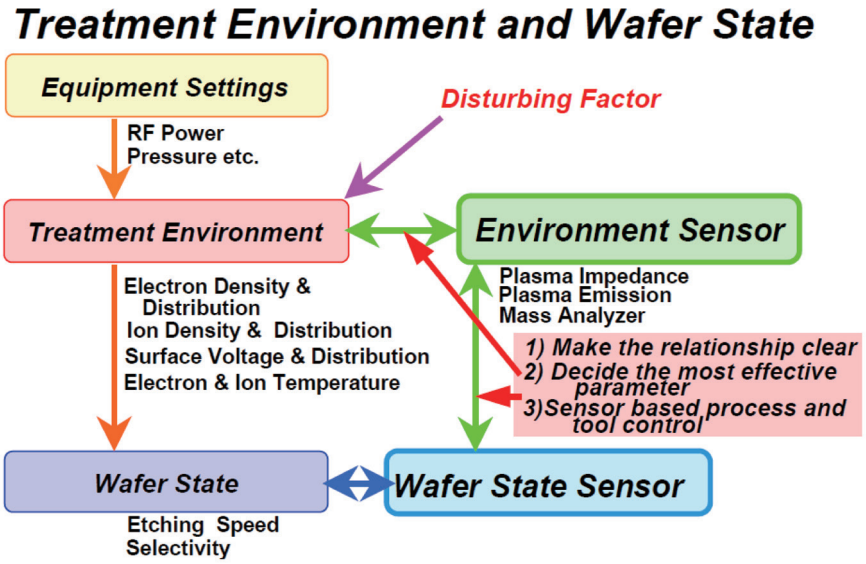

Figure 6 Treatment Environment and Wafer State in Dry Etch Process
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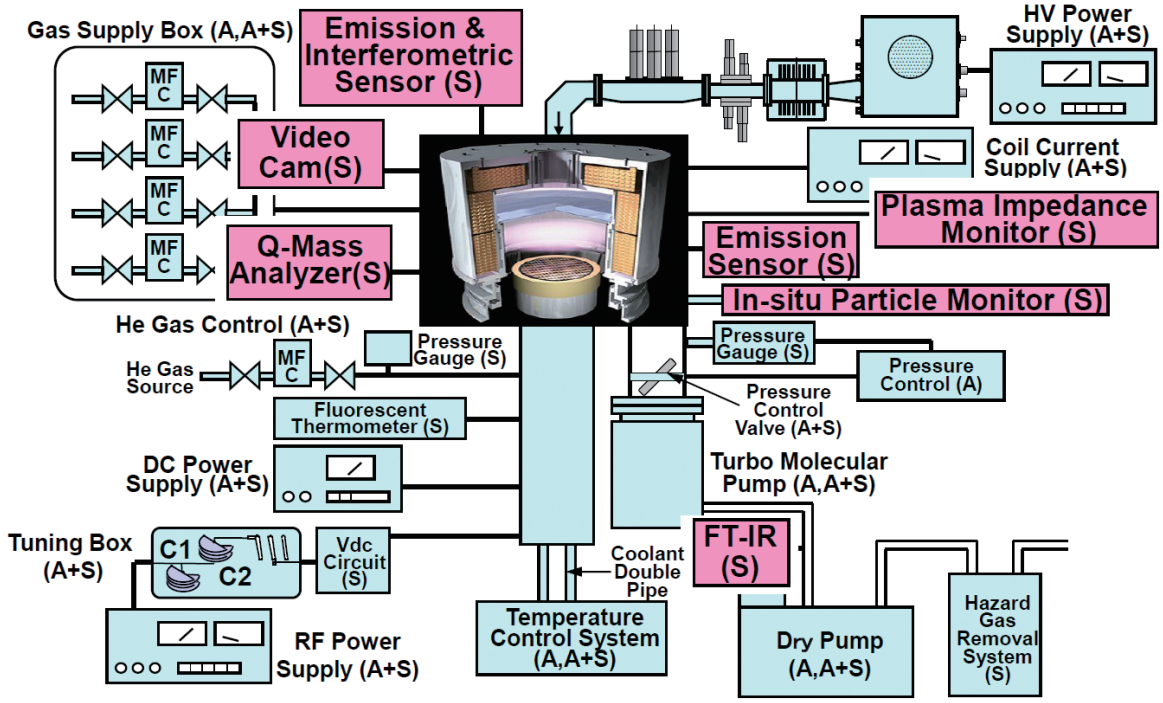

Figure 7 Candidate Sensing Functions in Dry Etch Tool
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generated in the reaction chamber, but has not been applied due to issues of sensor life and low scan speed. A product compatible with a low scan speed of 100 msec is now under development, which will probably be a valuable means of sensing in ALD and ALE processes.

(4) Plasma impedance monitor, or PIM: PIMs are mostly used for detecting abnormal values because the relationship with actual physical data can hardly be clarified. However, the technology may be usable for sensing chronological changes through data analysis and measurement modeling.

(5) Luminescent sensor (Emission sensor): This is presently the most used sensor, but its applications are limited. The device can also be used for sensing a specific type of light emission to provide feedback to process recipes, which is so-called run-to-run (R2R) control, and has been applied in volume production of wafers.

(6) Particle sensor (In-situ particle monitor): This type of sensing is hardly deemed applicable for recent devices because its minimum detectable particle size is about 0.2 μm. The sensor would be capable of detecting finer particles when combined with the condense nucleation method (CN); which will be effectively used if integrated into In-situ particle monitoring system.

(7) FT-IR: When installed in the exhaust system, the instrument can identify the reaction products generated and determine their quantity. The technology is expected to be used for determination of the end point in an ALE process, as well as cleaning.

Meanwhile, actuators such as gas flow control, radio frequency power supply, wafer cooling and so on also have sensing functions; so their effective application is also important for better supply stabilization.

The present and the future aspects of flow control technology

As mentioned above, flow control of the gas supplied for the purpose of process reaction is important in CVD/ALD and dry-etching, where thermal mass flow controllers (MFCs) are often used. After various issues concerning thermal MFCs came into focus with the progress of microscaling, there were moves to set the standards for flow control: in the 1990s, standardization of digital communications for sensor actuators including MFCs (E54) was carried out to ensure improved controllability and reduced cost. In the early 2000s, standardization of surface mount technology (F82 to F95) was conducted to establish the basis of downsizing and normalization of the gas supply system. In recent years, however, more and more process technologies, particularly ALD, have come to use liquids and solids with low vapor pressure. Basically, ALD is a reaction system relatively independent of the amount of the source supplied because it uses a self-limiting reaction. Nevertheless, there are many ALD processes that depend on the supply of the source, for the

purpose of pursuing mass productivity. Against this backdrop, development of high precision flow control technologies that are fully applicable for liquid and solid sources is becoming absolutely necessary in order to minimize the individual differences and chronological changes in each piece of equipment.

As the first step of the endeavor, flow calibration of the actual process gas (live gas) is now being studied. In reality, flow calibration for thermal MFCs is mostly carried out by feeding an inert gas such as N_2 instead of the gas that is used in the actual process, because the latter is usually highly reactive and could cause various problems when exposed to heat for the purpose of flow rate measurement.

$$Q_p = \mathrm{N} \cdot \frac{\mathrm{C_{pk}}}{\mathrm{C_{pp}}} \cdot Q_k \quad \cdots\cdots (1)$$

Where: Q_p = process gas flow rate,
Q_k = calibration gas flow rate,
N = compensation coefficient,
$\mathrm{C_{pp}}$ = molar specific heat of process gas at constant pressure,
$\mathrm{C_{pk}}$ = molar specific heat of calibration gas at constant pressure

The actual flow rate of the process gas is determined by Cpp, i.e. the molar specific heat of the process gas at constant pressure, and the compensation coefficient N. At this moment, the definition of Cpp is not unified among suppliers, with the compensation coefficient also varying due to different calibration methods adopted by suppliers, causing deviation from the actual flow rate. The method currently under study is based on a rate-of-rise (ROR) system, which is sometimes used for measurement of the actual flow rate of process gas. The measurement principle of the ROR system is as follows: First, the gas under control by an MFC is supplied to a vacuum-evacuated container. Then, the rate of pressure rise inside the container is obtained to calculate the flow rate with use of the state equation of the gas.

$$Q \propto \left(\frac{\Delta P}{\Delta t} \right) \cdot \frac{V}{T} \cdot \frac{1}{Z} \quad \cdots\cdots (2)$$

Where: Q = flow rate, ΔP = pressure rise,
Δt = time of pressure rise, V = container volume,
T = temperature, Z = compression coefficient

I hope that the second and third stages of the study will successfully establish the way of obtaining the desired gas flow rate regardless of the type of gas used.

Conclusion

CVD/ALD and dry-etching are key technologies for the production of semiconductor wafers in the future. They will be more and more frequently used and also required to have a wide range of capabilities. However, the equipment and process used with these technologies have not reached a sufficient level of perfection, still requiring various actions to be taken. Along with the further improvement of process sensing technology, advancement of gas flow rate control techniques is necessary. To realize this aim, equipment users, equipment suppliers, suppliers of functional components, and system software suppliers must join together to advance these development activities.